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IBM CORPORATION- AUSTIN (JVL)
C/O VAN LEEUWEN & VAN LEEUWEN
PO BOX 90609
AUSTIN, TX 78709-0609

EXAMINER	
IWASHKO, LEV	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/828,455	ACCAPADI ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/20/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C.103(a) as being unpatentable over Kissell (US Patent 7,017,025 B1), further in view of Lee et al. (US Patent 6,327,642 B1) and Cooksey et al. (US PG Pub 2003/0105940 A1).

Kissell teaches the following limitation of Claim 1.

Claim 1. A computer implemented method comprising:

- detecting that a memory being managed by a virtual memory manager is constrained; *(Column 6, lines 53-67 and Column 7, lines 1-5 State the following: "A system wide virtual memory scheme is considered beneficial in a unified memory SoC system for several reasons. First, having all processing elements working on the same unified memory implies that, without some form of memory management one processing element can corrupt the storage being used by another processing element. Second, some form of memory allocation scheme is desirable that can dynamically allocate the shared memory between the processing elements. A paged virtual memory system is considered appropriate because it can reduce or eliminate problems of memory fragmentation, and allow forms of demand paging. Third, by placing a virtual memory structure between a processing element and memory, the effective addressing range can be expanded for a processing element with a constrained logical/physical address space. The amount of memory addressable at any one time remains the same, but by changing the virtual memory mapping underneath the native logical/physical address space, that constrained address space can be made into a changeable "window" into a larger memory")*

Kissell's invention differs from the claimed invention in that there is no specific

reference to dynamic setting alteration.

Kissell fails to teach the entirety of Claim 1. However, Lee teaches the following aspect of Claim 1:

- and dynamically altering settings *(Column 9, lines 46-61 – State the following: "Operation of memory system 300 proceeds as follows. Initially, the external processing system which is coupled to system bus 315 determines which memory masters will access which virtual access channels. That is, the external processing system assigns each memory master to one or more of the virtual access channels. Each virtual access channel is accessed by one or more external memory masters. These assignments are determined by the memory controller logic, the system BIOS, or the memory management manager part of the operating system. The assignments may be static (i.e., never change once assigned), or dynamic (i.e., the memory manager juggles the virtual channel assignments as the system resources change). The virtual channels can be assigned as needed by the system processors")*

Kissell's and Lee's inventions differ from the claimed invention in that there is no specific reference to a read ahead process.

Kissell and Lee fail to teach the entirety of Claim 1. However, Cooksey teaches the following aspect of Claim 1:

- used by a sequential access read ahead process in response to the detection, wherein the altered settings are adapted to conserve memory used by the sequential access read ahead process. *(Section 0093, lines 5-9 – State the following: "The scan threshold will be less than or equal to the threshold request depth. For example, where the threshold request depth is three (3), the scan threshold could be two (2). Similarly, where the threshold request depth is five (5), the scan threshold could be three (3). Efficiency considerations also play a role in selection of the scan threshold, as the scan threshold delays reinforcement until a prefetch chain has been traversed to a request depth equal to the scan threshold, thereby conserving memory resources")*

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Mechanism for Proxy Management of Multiprocessor Virtual Memory" of Kissell, Lee's

"Parallel Access Virtual Channel Memory System" and Cooksey's "Method and Apparatus for Reinforcing a Prefetch Chain" before him at the time the invention was made, to combine the inventions to so that the system would run efficiently.

3. Claim 2 is rejected under 35 U.S.C.103(a) as being unpatentable over Kissell (US Patent 7,017,025 B1) as applies to Claim 1, further in view of Lee et al. (US Patent 6,327,642 B1), Cooksey et al. (US PG Pub 2003/0105940 A1) and Frandeen (US Patent 5,606,685 A).

Kissell, Lee, and Cooksey teach the limitations of Claim 1.

Kissell, Lee, and Cooksey's inventions differ from the claimed invention in that there is no reference to decreasing a maximum page ahead value.

Kissell, Lee, and Cooksey fail to teach Claim 2, which discloses: "The method of claim 1 wherein the altering further comprises: decreasing a maximum page ahead value, wherein the maximum page ahead value corresponds to a maximum number of pages read by the sequential access read ahead process." However, Frandeen states the following: "A method of controlling paging on a workstation capable of concurrently running a plurality of applications, said method comprising the steps of: providing a workstation memory; dividing said workstation memory into a plurality of pages having files stored therein; maintaining a page table for each running application indicating corresponding files and pages and also whether each page is present; providing non-volatile storage for storing not present pages; assigning pages of said workstation memory to each running application; providing a page fault when a running application requests access to a page which said page table indicates is not present; determining whether a free page is available for storing the not present page of the page faulting application; when a free page is determined to be available to store the not present page, then examining the page table of the

page faulting application with respect to adjacent pages both preceding and following the not present page which caused the page fault; selecting as candidate pages for prefaulting consecutive not present adjacent pages both following and preceding said not present page which are also from the same file as the not present page; searching said workstation memory to find an available block of contiguous pages for storing the not present page and the adjacent candidate pages; and reading in from said non-volatile storage the not present page which produced the page fault and the maximum number of adjacent candidate pages that can be accommodated by the block found by said searching. 2. The method of claim 1, including the step of selectively providing a prefetching capability for a running application, and wherein the steps of examining, selecting, searching and reading are performed for an application when the application has been provided with a prefaulting capability. 3. The method of claim 1, including the step of: when the step of examining does not find any candidate pages for prefaulting, then reading the not present page from said non-volatile storage into the free page found by said determining without performing the steps of selecting and searching. 4. The method of claim 1, including the step of limiting said candidate pages to a predetermined maximum number. 5. The method of claim 4, wherein said predetermined maximum number is chosen based on the maximum number of pages which can be read from said non-volatile storage during a reading operation. 6. The method of claim 4, wherein the step of limiting chooses candidate pages for prefaulting such that candidate pages following the not present page are chosen ahead of those preceding the not present page" (Column 18, lines 19-67 and Column 19, lines 1-8).

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Mechanism for Proxy Management of Multiprocessor Virtual Memory" of Kissell, Lee's

"Parallel Access Virtual Channel Memory System", Cooksey's "Method and Apparatus for Reinforcing a Prefetch Chain" and Frandeen's "Computer Workstation Having Demand-Paged Virtual Memory and Enhanced Prefaulting" before him at the time the invention was made, to combine the inventions to decrease the maximum page value to avoid overflow, thereby maximizing system performance.

4. Claim 3 is rejected under 35 U.S.C.103(a) as being unpatentable over Kissell (US Patent 7,017,025 B1) as applies to Claim 2, further in view of Lee et al. (US Patent 6,327,642 B1), Cooksey et al. (US PG Pub 2003/0105940 A1), Frandeen (US Patent 5,606,685 A) and Campbell et al. (US Patent 6,408,313 B1).

Kissell, Lee, Cooksey, and Frandeen teach the limitations of Claim 2.

Kissell, Lee, Cooksey, and Frandeen's inventions differ from the claimed invention in that there is no reference to decreasing a maximum page ahead value by a difference between the number of free pages and a minimum constant.

Kissell, Lee, Cooksey, and Frandeen fail to teach Claim 3, which discloses: "The method of claim 2 further comprising: retrieving a value corresponding to a number of free page frames currently being managed by the virtual memory manager; and calculating a difference between the number of free page frames value and a minimum desired free page constant, wherein the maximum page ahead value is decreased by an amount based on the calculated difference." However, Campbell states the following: "When the operating system returns with a representation of the number of free pages available for applications, the lazy writer thread determines the length of this list and then determine whether committed memory for the application should grow or shrink. It sets a target number to reach by taking the current size and

subtracting 5M in one embodiment. By selecting a threshold of 5M, an excess of 1M (5M-4M) is created which allows other applications to use memory without necessarily forcing the operating system into paging. If negative, as determined at block 320, an estimate of the number of pages to give back, or decommit is made at 325. A target size is then set at 330 and provided to memory management of the application. If the free list size is greater than 5M as determined at 340, an estimate is made of how much more memory can be committed to the application at 345 and the target is adjusted or modified at 350 and provided to the memory management of the application. After the target is modified, either made smaller or larger at 330 and 350 respectively, the thread returns to 310 to wake up again later" (Column 6, lines 30-49).

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Mechanism for Proxy Management of Multiprocessor Virtual Memory" of Kissell, Lee's "Parallel Access Virtual Channel Memory System", Cooksey's "Method and Apparatus for Reinforcing a Prefetch Chain", Frandeen's "Computer Workstation Having Demand-Paged Virtual Memory and Enhanced Prefaulting" and Campbell's "Dynamic Memory Allocation Based on Free Memory Size" before him at the time the invention was made, to combine the inventions to decrease the maximum page value by a difference between the number of free pages and a minimum constant to have uniformity throughout the system, thereby maximizing system performance.

5. Claim 5 is rejected under 35 U.S.C.103(a) as being unpatentable over Kissell (US Patent 7,017,025 B1) as applies to Claim 1, further in view of Lee et al. (US Patent 6,327,642 B1) and Cooksey et al. (US PG Pub 2003/0105940 A1).

Kissell and Lee teach the limitations of Claim 1.

Kissell and Lee's inventions differ from the claimed invention in that there is no reference to disabling the read ahead process.

Kissell and Lee fail to teach Claim 5, which discloses: "The method of claim 1 wherein the altering further comprises: disabling the sequential access read ahead process." However, Cooksey states the following: "The prefetch chain may be terminated" (Section 0073, lines 4-5).

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Mechanism for Proxy Management of Multiprocessor Virtual Memory" of Kissell, Lee's "Parallel Access Virtual Channel Memory System" and Cooksey's "Method and Apparatus for Reinforcing a Prefetch Chain" before him at the time the invention was made, to combine the inventions to allow for the read ahead process to be terminated, so that the system would not run in an infinite loop.

6. Claim 7 is rejected under 35 U.S.C.103(a) as being unpatentable over Kissell (US Patent 7,017,025 B1), further in view of Lee et al. (US Patent 6,327,642 B1), Cooksey et al. (US PG Pub 2003/0105940 A1), Frandeen (US Patent 5,606,685 A) and Campbell et al. (US Patent 6,408,313 B1).

Campbell teaches the following limitation of Claim 7.

> A computer-implemented method of managing memory pages, wherein the memory includes a number of used pages and a number of free pages, said method comprising:
> - retrieving a freelist value corresponding to the current number of free pages; determining that the freelist value is less than a predetermined minimum value; *(Column 6, lines 30-49 – State the following "When the operating system returns with a representation of the number of free pages available for applications, the lazy writer thread determines the length of this list and then determine whether committed memory for the application should grow or shrink. It sets a target number to reach by taking the current size and subtracting 5M in one embodiment. By selecting a threshold of 5M, an excess of 1M (5M-*

4M) is created which allows other applications to use memory without necessarily forcing the operating system into paging. If negative, as determined at block 320, an estimate of the number of pages to give back, or decommit is made at 325. A target size is then set at 330 and provided to memory management of the application. If the free list size is greater than 5M as determined at 340, an estimate is made of how much more memory can be committed to the application at 345 and the target is adjusted or modified at 350 and provided to the memory management of the application. After the target is modified, either made smaller or larger at 330 and 350 respectively, the thread returns to 310 to wake up again later")

Campbell's invention differs from the claimed invention in that there is no specific reference to dynamic setting alteration.

Campbell fails to teach the entirety of Claim 7. However, Lee teaches the following aspect of Claim 7:

- and dynamically altering settings *(Column 9, lines 46-61 – State the following: "Operation of memory system 300 proceeds as follows. Initially, the external processing system which is coupled to system bus 315 determines which memory masters will access which virtual access channels. That is, the external processing system assigns each memory master to one or more of the virtual access channels. Each virtual access channel is accessed by one or more external memory masters. These assignments are determined by the memory controller logic, the system BIOS, or the memory management manager part of the operating system. The assignments may be static (i.e., never change once assigned), or dynamic (i.e., the memory manager juggles the virtual channel assignments as the system resources change). The virtual channels can be assigned as needed by the system processors")*

Compbell and Lee's inventions differ from the claimed invention in that there is no specific reference to a read ahead process.

Campbell and Lee fail to teach the entirety of Claim 7. However, Cooksey teaches the following aspect of Claim 7:

- used by a sequential access read ahead process in response to the detection, wherein the altered settings are adapted to decrease the

allocation of free pages to the sequential access read ahead process. *(Section 0093, lines 5-9 – State the following: "The scan threshold will be less than or equal to the threshold request depth. For example, where the threshold request depth is three (3), the scan threshold could be two (2). Similarly, where the threshold request depth is five (5), the scan threshold could be three (3). Efficiency considerations also play a role in selection of the scan threshold, as the scan threshold delays reinforcement until a prefetch chain has been traversed to a request depth equal to the scan threshold, thereby conserving memory resources")*

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Mechanism for Proxy Management of Multiprocessor Virtual Memory" of Kissell, Lee's "Parallel Access Virtual Channel Memory System", Cooksey's "Method and Apparatus for Reinforcing a Prefetch Chain", Frandeen's "Computer Workstation Having Demand-Paged Virtual Memory and Enhanced Prefaulting" and Campbell's "Dynamic Memory Allocation Based on Free Memory Size" before him at the time the invention was made to combine the inventions to so that the system would run efficiently.

7. Claims 11 and 13 are rejected under 35 U.S.C.103(a) as being unpatentable over Kissell (US Patent 7,017,025 B1) as applies to Claims 7-8, further in view of Lee et al. (US Patent 6,327,642 B1), Cooksey et al. (US PG Pub 2003/0105940 A1), Frandeen (US Patent 5,606,685 A) and Campbell et al. (US Patent 6,408,313 B1).

Kissell, Lee, Cooksey, Frandeen, and Campbell all teach the limitations of claims 7-8.

The Claims are stated as follows:

Claim 11. The method of claim 8 further comprising: executing a virtual memory manager for a time interval following the decreasing, wherein the virtual memory manager manages the memory pages and wherein the virtual memory manager includes the sequential access read ahead process; retrieving a subsequent freelist value corresponding to the number of free pages available after the time interval; comparing the subsequent freelist

value with the current maximum page ahead value; and disabling the sequential access read ahead process in response to the comparison.

Claim 13. The method of claim 8 further comprising: executing a virtual memory manager for a time interval following the decreasing, wherein the virtual memory manager manages the memory pages and wherein the virtual memory manager includes the sequential access read ahead process; retrieving a subsequent freelist value corresponding to the number of free pages available after the time interval; determining that the subsequent freelist value is greater than the predetermined minimum value; and setting the current maximum read ahead value equal to the constant maximum page ahead value in response to the determination.

Kissell, Lee, Cooksey, Frandeen, and Campbell's inventions differ from the claimed invention in that they do not explicitly state that anything is done for a time interval. However, it is obvious to anyone skilled in the art that anything that requires execution needs to be executed within a certain time interval. There has been no specification as to how long the proposed time interval should be. Therefore, Claims 11 and 13 remain rejected under 103(a).

8. Claim 15 is rejected under 35 U.S.C.103(a) as being unpatentable over Kissell (US Patent 7,017,025 B1) as applies to Claims 7-8, further in view of Lee et al. (US Patent 6,327,642 B1), Cooksey et al. (US PG Pub 2003/0105940 A1), Frandeen (US Patent 5,606,685 A), Campbell et al. (US Patent 6,408,313 B1) and Narayanan (US PG Pub 2004/0268124 A1).

Kissell teaches the following limitations of Claim 15.

Claim 15. An information handling system comprising:

- one or more processors; a memory accessible by the processors; an operating system that controls the processors; *(Column 4, lines 64-67 – State the following: "The proxy processor 304 is used to execute general system management instructions (operating system instructions) for the system-on-a-chip (SoC) that includes the processing elements 306 and the proxy caches 308")*
- a virtual memory manager, included with the operating system, that manages use of the memory; *(Column 6, lines 53-67 and Column 7, lines 1-5 State the following: "A system wide virtual memory scheme is considered beneficial in a unified memory SoC system for several reasons. First, having all processing elements working on the same*

unified memory implies that, without some form of memory management one processing element can corrupt the storage being used by another processing element. Second, some form of memory allocation scheme is desirable that can dynamically allocate the shared memory between the processing elements. A paged virtual memory system is considered appropriate because it can reduce or eliminate problems of memory fragmentation, and allow forms of demand paging. Third, by placing a virtual memory structure between a processing element and memory, the effective addressing range can be expanded for a processing element with a constrained logical/physical address space. The amount of memory addressable at any one time remains the same, but by changing the virtual memory mapping underneath the native logical/physical address space, that constrained address space can be made into a changeable "window" into a larger memory")

- memory conservation software used by the virtual memory manager, the software effective to: *(Column 9, lines 5-8 – State the following: "In addition to implementations of the invention using hardware, the invention can be embodied in computer readable program code (e.g., software)")*
- detect that a memory being managed by a virtual memory manager is constrained; *(Column 6, lines 53-67 and Column 7, lines 1-5 State the following: "A system wide virtual memory scheme is considered beneficial in a unified memory SoC system for several reasons. First, having all processing elements working on the same unified memory implies that, without some form of memory management one processing element can corrupt the storage being used by another processing element. Second, some form of memory allocation scheme is desirable that can dynamically allocate the shared memory between the processing elements. A paged virtual memory system is considered appropriate because it can reduce or eliminate problems of memory fragmentation, and allow forms of demand paging. Third, by placing a virtual memory structure between a processing element and memory, the effective addressing range can be expanded for a processing element with a constrained logical/physical address space. The amount of memory addressable at any one time remains the same, but by changing the virtual memory mapping underneath the native logical/physical address space, that constrained address space can be made into a changeable "window" into a larger memory")*

Kissell's invention differs from the claimed invention in that there is no specific reference to disk swap area.

Kissell fails to teach the entirety of Claim 15. However, Narayanan teaches the following aspect of Claim 15:

- a nonvolatile storage area managed by the operating system and including a disk swap area used by the virtual memory manager; *(Section 0008, lines 1-19 – State the following: "As an example of an application performing security services consider a virtual memory manager (VMM) application. In computing and storage, VMM applications are used to swap a portion of the process space to/from memory (this portion of memory oftentimes referred to as a swap disk) when an application performing security services is in use and requests a page fault. Without security services, if the memory, which may be embodied in a hard disk, is stolen, the cryptographic keys used to perform the security services may be retrieved, such as by performing reverse engineering techniques. To avoid exposing the cryptographic keys to such breaches, swap operations may be combined with encryption/decryption functions so that the data stored in the swap disk is secured. As another example, consider a CFS application, which may perform operations similar to VMM applications in either real or non-real time. As can be shown, the policies and parameters for many applications are different, but all provide the same set of services (e.g., secured storage)")*

Kissell and Narayanan's invention differs from the claimed invention in that there is no specific reference to dynamic setting alteration.

Kissell and Narayanan fails to teach the entirety of Claim 15. However, Lee teaches the following aspect of Claim 15:

- and dynamically altering settings *(Column 9, lines 46-61 – State the following: "Operation of memory system 300 proceeds as follows. Initially, the external processing system which is coupled to system bus 315 determines which memory masters will access which virtual access channels. That is, the external processing system assigns each memory master to one or more of the virtual access channels. Each virtual access channel is accessed by one or more external memory masters. These assignments are determined by the memory controller logic, the system BIOS, or the memory management manager part of the operating system. The assignments may be static (i.e., never change once assigned), or dynamic (i.e., the memory manager juggles*

the virtual channel assignments as the system resources change). The virtual channels can be assigned as needed by the system processors")

Kissell, Narayanan and Lee's inventions differ from the claimed invention in that there is no specific reference to a read ahead process.

Kissell, Narayanan and Lee fail to teach the entirety of Claim 15. However, Cooksey teaches the following aspect of Claim 15:

- a sequential access read ahead process performed by the operating system adapted to pre-fetch data being sequentially read from file stored in the nonvolatile storage area; used by a sequential access read ahead process in response to the detection, wherein the altered settings are adapted to conserve memory used by the sequential access read ahead process. *(Section 0093, lines 5-9 – State the following: "The scan threshold will be less than or equal to the threshold request depth. For example, where the threshold request depth is three (3), the scan threshold could be two (2). Similarly, where the threshold request depth is five (5), the scan threshold could be three (3). Efficiency considerations also play a role in selection of the scan threshold, as the scan threshold delays reinforcement until a prefetch chain has been traversed to a request depth equal to the scan threshold, thereby conserving memory resources")*

It would have been obvious to one of ordinary skill in the art, having the teachings of the "Mechanism for Proxy Management of Multiprocessor Virtual Memory" of Kissell, Narayanan's "Systems and Methods for Creating and Maintaining a Centralized Key Store", Lee's "Parallel Access Virtual Channel Memory System" and Cooksey's "Method and Apparatus for Reinforcing a Prefetch Chain" before him at the time the invention was made, to combine the inventions to so that the system would run efficiently.

9. Claim 29 is rejected on the same bases as Claim 1, as they share nearly identical limitations with only their preambles differing.

10. Claims 8, 16, 22, 30, and 36 are rejected on the same basis as Claim 2, as they share nearly identical limitations with only their preambles differing.

11. Claims 18 and 32 are rejected on the same bases as Claim 3, as they share nearly identical limitations with only their preambles differing.

12. Claims 14, 19, 28, 33, and 42 are rejected on the same basis as Claim 5, as they share nearly identical limitations with only their preambles differing.

13. Claim 35 is rejected on the same bases as Claim 7, as they share nearly identical limitations with only their preambles differing.

14. Claims 25 and 39 are rejected on the same bases as Claim 11, as they share nearly identical limitations with only their preambles differing.

15. Claims 27 and 41 are rejected on the same bases as Claim 13, as they share nearly identical limitations with only their preambles differing.

16. Claim 21 is rejected on the same bases as Claim 15, as they share nearly identical limitations with only their preambles differing.

17. Claims 4, 6, 9-10, 12, 18, 20, 23-24, 26, 32, 34, 37-38, and 40 are all rejected due to their dependence on claims that have already been rejected. If the aforementioned claims were written in independent form, keeping in line with the limitations set forth in the claims upon which they depend, then the claims would indeed be novel.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

PIERRE BATAILLE
PRIMARY EXAMINER
4|29|06